

FIG. 1

**Prior Art**

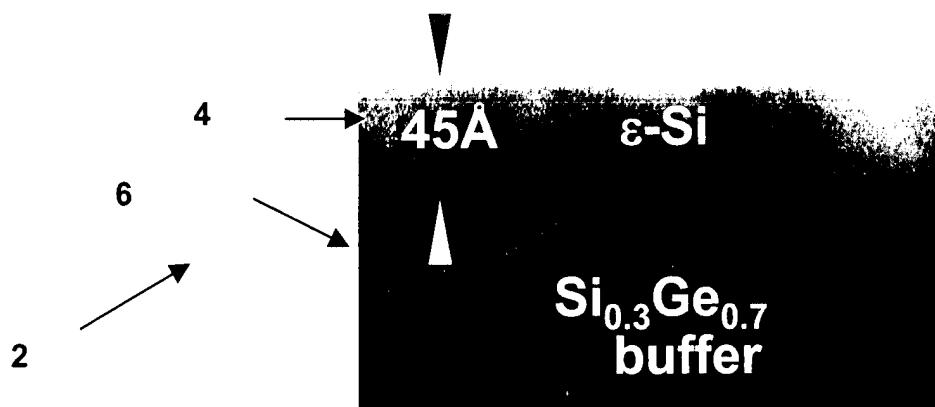


FIG. 2A

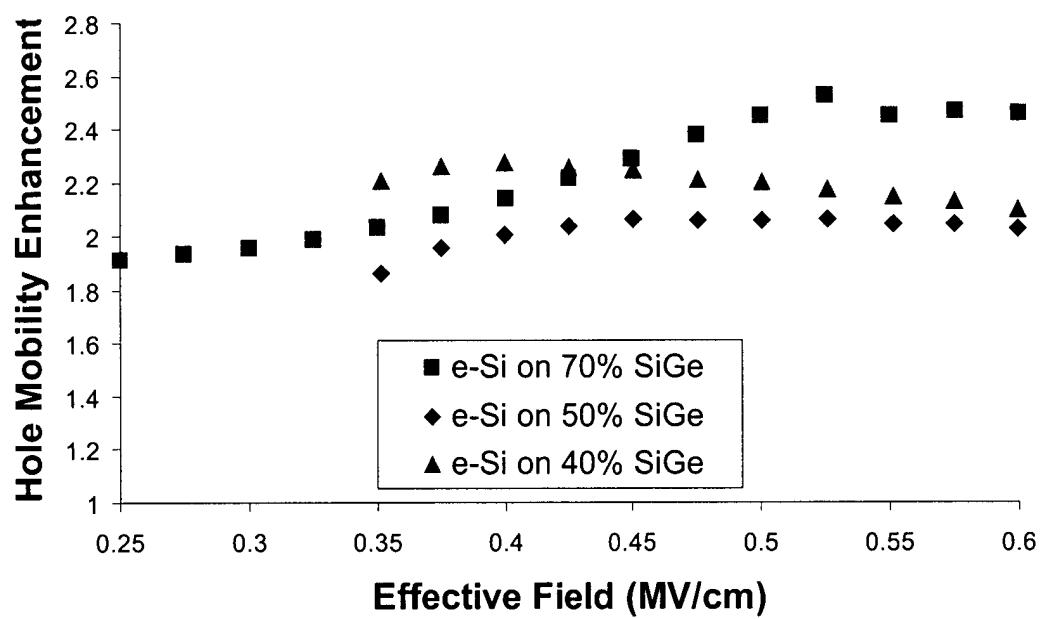
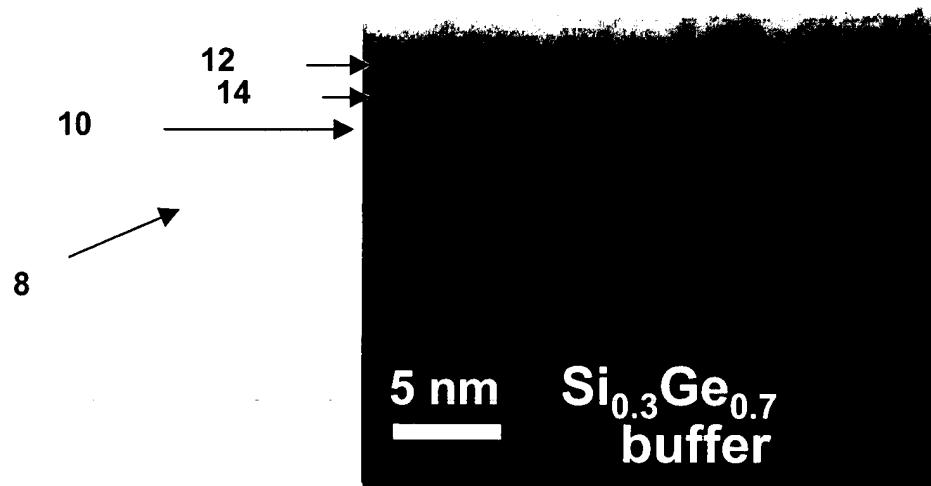
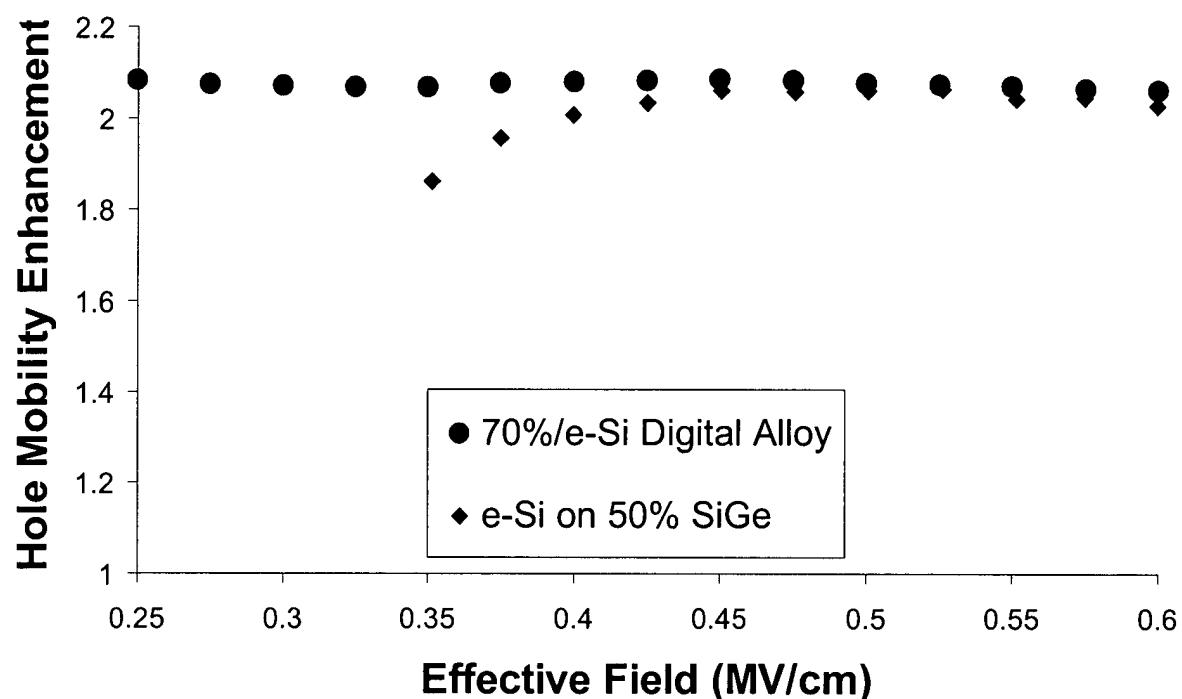


FIG. 2B

**Bright layers are  $\varepsilon$ -Si  
Dark layers are  $\text{Si}_{0.3}\text{Ge}_{0.7}$**



**FIG. 3A**



**Figure 3b- Mobility enhancement of  $\varepsilon$ -Si/ $\text{Si}_{0.3}\text{Ge}_{0.7}$  digital alloy pMOSFET compared to conventional  $\varepsilon$ -Si device**